## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Nace Layadi, et al.

Serial No.:

N/A

Filed:

Herewith

For:

A TRENCH ISOLATION STRUCTURE AND METHOD

OF MANUFACTURE THEREFOR

Group No.:

N/A

**Examiner:** 

N/A

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

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Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents, publications and other information herein are listed below and on the attached Form PTO-1449. Copies of the listed references are submitted herewith.

## Reference:

Choices and Challenges for Shallow Trench Isolation; http://www.reed-electronics.com/semiconductor/index.asp?layout=articlePrint&articleID=C

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.

Respectfully submitted,

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Date: 19-03

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Substitute for form 1449/PTO				Complete if Known		
3-				Application Number	N/A	
INF	ORMATION	DIS	CLOSURE	Filing Date	Herewith	
(Use as many sheets as necessary)				First Named Inventor	Nace Layadi, et al.	
				Art Unit	N/A	
				Examiner Name	N/A	
Sheet	1	of	1	Attorney Docket Number	LAYADI 36-39	

NON PATENT LITERATURE DOCUMENTS							
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>				
		Choices and Challenges for Shallow Trench Isolation; http://www.reed-electronics.com/semiconductor/index.asp?layout=articlePrint&articleID=C					
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